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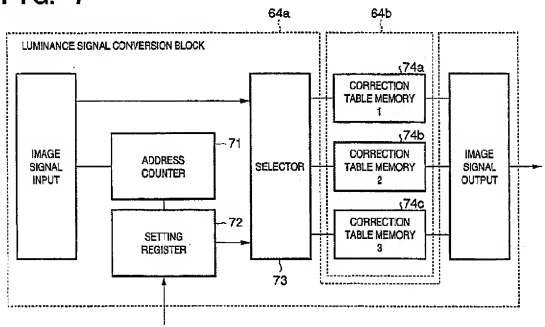
(54) Processing of signals from an image sensor consisting of a plurality of sensor areas

(57) An image processing apparatus includes an image sensor formed from a plurality of areas each including a plurality of pixels, and a corrector adapted to correct signals from the plurality of areas of the image sensor. The corrector has a plurality of correction data smaller in number than the areas, and performs correction by selectively using the correction data for each area of the image sensor.

FIG. 7



EP 1 289 265 A2

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to an image processing apparatus having an image sensing apparatus and a correction method and, more particularly, to an image processing apparatus in which an image sensing apparatus has a plurality of areas each including a plurality of pixels and processes signals output from the plurality of areas, and a correction method.

BACKGROUND OF THE INVENTION

[0002] Contact image sensors (CISs) have recently been developed and put into practical use along with reductions in size and weight in a scanner apparatus for inputting an image to a personal computer and the document reader of a facsimile apparatus. The contact image sensor is formed from a light source, rod lenses which implement a ×1 erect optical system, and a one-dimensional light-receiving sensor whose effective width is substantially the same as the maximum width of a document to be read. The CIS can shorten the optical path length of an optical system, compared to an optical system which uses a lens called a reduction optical system to reduce the main scanning width of a document to be read to a fraction of the original width and reads the image by a one-dimensional CCD sensor or the like. Accordingly, the CIS can implement a small-size, lightweight document reader.

[0003] With the recent advance in semiconductor process and production technique, CISs have been adopted in A4-size consumer scanners. With low cost and a small light quantity from a light source, the use of CISs in high-speed image reading apparatuses such as a copying machine is also being examined.

[0004] A CIS requires a length equal to the width of a document image in reading an image. Forming a sensor with this length from one sensor chip is less advantageous in terms of the technique and cost. The CIS generally ensures a reading length equal to the document image width by arraying a plurality of sensor chips.

[0005] In a copying machine using a CCD image sensor, a CCD image sensor which is divided into two blocks at the center and reads out signals from the two ends in order to cope with a high-speed copying machine has been studied.

[0006] In the CIS, the plurality of sensor chips are linearly arrayed, as described above. Image signals from the sensor chips undergo well-known shading correction to adjust their black and white levels. The white level is generally adjusted by pixel, and the black level is adjusted by chip, pixel, or the like, which are both known well. The known shading correction is a reading correction method which assumes an ideal linearity of a read image signal. If the linearity characteristics of the chips of a multi-chip vary, the image signal level also varies at the halftone level. The density is different between adjacent chips, seriously degrading the quality.

[0007] Even if the black and white levels are adjusted by known shading correction in the CCD image sensor which is divided into two blocks at the center and reads out signals from the two ends, the linearity characteristic varies between the right and left sides due to differences in read characteristics at the two ends and the characteristics of a plurality of amplifiers. The levels of read signals differ from each other at the halftone level, resulting in a density difference and serious degradation in image quality. The density difference and quality degradation are conspicuous at the central boundary.

[0008] In general, these problems of the above-mentioned CCD image sensor have been solved by performing linearity correction using an LUT (Look Up Table) stored in a known ROM or RAM.

[0009] An LUT can realize arbitrary signal conversion by supplying an input signal as an address and reading out data stored at the address as an output signal. When the number of signals to be corrected is small, the correction method by signal conversion using the LUT is an ideal correction method.

[0010] However, when the correction method using the LUT is directly used in a color CIS with an array of 16 sensor chips, 16 chip × 3 colors = a total of 48 LUTs are required. This leads to an impractically large-scale circuit regardless of whether the LUTs are constituted by discrete memories or incorporated in an ASIC.

[0011] When the conventional ODD/EVEN output (i.e., odd- and even-numbered pixels are read using different reading systems) is executed from two ends in a CCD image sensor which reads out signals from two ends, a monochrome image requires four LUTs, and a color image requires 12 LUTs, which is three times the number of LUTs for a monochrome image. A large number of LUTs cannot be ignored, either.

[0012] In short, output variations of a plurality of systems with different linearity characteristics that cannot be completely corrected by known shading correction, e.g., halftone linearity variations of a plurality of chips, blocks, or output systems with different characteristics are closed up as a result of implementing the multi-chip of a CIS or multi-read of a high-speed CCD. Especially for a color image, difficulty lies three times.

[0013] At present, the reader of a copying machine or the like is normally OFF for power saving and low power consumption. Even if the user wants to activate the copying machine and read a document as quickly as possible, a time of about 5 sec is taken for calculating LUT curves and writing the curves to RAM by the CPU even in the use of the simplest straight line in an arrangement where LUTs are prepared for the number of chips, blocks, or output systems subjected to linearity correction. Also from this viewpoint, the use of many LUTs is undesirable.

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SUMMARY OF THE INVENTION

[0014] According to the present invention, an image processing apparatus is characterized by comprising: an image sensor formed from a plurality of areas each including a plurality of pixels; and a corrector adapted to correct signals output from the plurality of areas of the image sensor, wherein the corrector has a plurality of correction data smaller in number than the areas, and performs correction by selectively using any one of the plurality of correction data for each area of the image sensor.

[0015] According to the present invention, an image processing apparatus is characterized by comprising: an image sensor formed from a plurality of areas each including a plurality of pixels; a corrector adapted to correct signals from the plurality of areas of the image sensor; and a density reference member having a white reference area and a halftone gray reference area, wherein the corrector has a plurality of correction data smaller in number than the areas of a sensor chip, and executes first correction of performing shading correction on the basis of a signal obtained by reading the white reference area by the image sensor, and second correction (64a) of performing correction by selectively using the correction data for each area of the image sensor on the basis of a signal obtained by reading the halftone gray reference area by the image sensor.

[0016] Further, an image processing apparatus is characterized by comprising: an image sensor formed from a plurality of areas each including a plurality of pixels; and a corrector adapted to correct linearity of signals output from the plurality of areas, wherein the corrector includes: a multiplier which multiplies the signals output from the plurality of areas by a coefficient; and an adder which adds a coefficient to the signals output from the plurality of areas.

[0017] Furthermore, a correction method of correcting image data obtained from an image sensor formed from a plurality of areas each including a plurality of pixels, is characterized by comprising the steps of: reading a predetermined halftone image by the image sensor; selecting one of a plurality of correction data smaller in number than the plurality of areas for each of the plurality of areas on the basis of a signal level of the read image; storing correspondences between the plurality of areas and selected correction data; determining which of the areas outputs image data from the image sensor; and performing correction using correction data corresponding to the determined area.

[0018] Further, a correction method of correcting image data obtained from an image sensor formed from a plurality of areas each including a plurality of pixels is characterized by comprising the steps of: reading a predetermined halftone image by the image sensor; calculating a coefficient set used for correction for each of the plurality of areas on the basis of a signal level of the read image; storing correspondences between the plurality of areas and calculated coefficient sets; determining which of the areas outputs image data from the image sensor; selecting one of the stored coefficient sets on the basis of the determined area and the signal level of the image data; and correcting signals output from the plurality of areas by using coefficients of the selected coefficient set, wherein the correcting step includes: a step of multiplying the signals output from the plurality of areas by the coefficients of the selected coefficient set; and a step of adding the coefficients of the selected coefficient set to the signals output from the plurality of areas.

[0019] Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Fig. 1 is a schematic view showing the image reader of an image processing apparatus according to a first embodiment of the present invention;
Fig. 2 is a perspective view showing the arrangement of part of a contact image sensor;
Fig. 3 is a block diagram showing the arrangement of a multi-chip sensor;
Fig. 4 is a block diagram mainly showing the arrangement of the image processor of the image processing apparatus according to the first embodiment of the present invention;
Fig. 5 is a block diagram showing the arrangement of part of the image processing apparatus according to the first embodiment of the present invention;
Fig. 6 is a block diagram showing the arrangement of an image processing circuit according to the first embodiment of the present invention;
Fig. 7 is a block diagram showing the arrangement of a luminance signal conversion block according to the first embodiment of the present invention;
Fig. 8 is a view showing a density reference plate;
Figs. 9A to 9C are graphs showing examples of the characteristic of a correction table according to the first embodiment of the present invention;
Fig. 10 is a block diagram showing the arrangement of an image processing apparatus according to a second embodiment of the present invention;
Fig. 11 is a conceptual view showing a multi-chip sensor according to the second embodiment of the present invention;
Fig. 12 is a view showing the arrangement of a CIS;
Fig. 13 is a perspective view showing the CIS in Fig.

EP 1 289 265 A2 (1289265A2 | >)

12;

Fig. 14 is a schematic view showing the arrangement of one sensor chip which constitutes the multi-chip sensor according to the second embodiment of the present invention;

Figs. 15A and 15B are a graph and table for explaining linearity correction according to the second embodiment of the present invention;

Fig. 16 is a block diagram showing details of a linearity correction unit according to the second embodiment of the present invention;

Fig. 17 is a timing chart showing the driving and output of the multi-chip sensor according to the second embodiment of the present invention;

Fig. 18 is a block diagram showing a shading correction unit according to the second embodiment of the present invention;

Fig. 19 is a timing chart for explaining the output timing of a sorted image signal according to the second embodiment of the present invention;

Fig. 20 is a schematic view showing an image forming apparatus in which the image processing apparatus is mounted according to the second embodiment of the present invention;

Fig. 21 is a block diagram showing the arrangement of an image processing apparatus according to the third embodiment of the present invention;

Fig. 22 is a block diagram showing the concept of a center-division two-end-read type CCD image sensor;

Fig. 23 is a timing chart for explaining the output timing of a sorted image signal according to the third embodiment of the present invention;

Fig. 24 is a schematic view showing an image forming apparatus in which the image processing apparatus is mounted according to the third embodiment of the present invention;

Fig. 25 is a flow chart showing processing of selecting a correction table used in a sensor chip according to the first embodiment of the present invention;

Fig. 26 is a flow chart showing linearity correction processing according to the first embodiment of the present invention;

Fig. 27 is a flow chart showing processing of calculating a correction coefficient used in a sensor chip according to the second embodiment of the present invention; and

Fig. 28 is a flow chart showing linearity correction processing according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Preferred embodiments of the present invention will be described in detail in accordance with the accompanying drawings.

(First Embodiment)

[0022] The arrangement of the image reader of an image processing apparatus according to the first embodiment will be described with reference to Fig. 1.

[0023] Reference numeral 1 denotes a platen glass on which a document is set; 2, a platen cover which presses the platen glass and can be opened/closed; 3, a document set on the platen glass; 4, a contact image sensor (to be referred to as a "CIS" hereinafter) serving as a scanning optical system for reading the image of the document 3; 5, a carriage which holds the CIS; 9, a shaft serving as a guide when the carriage is moved in the sub-scanning direction in reading a document; 8, a timing belt fixed to the carriage 5; 6 and 7, pulleys which are arranged at the two ends of the timing belt so as to smoothly move the timing belt 8; 10, a stepping motor which is connected to either the pulley 6 or 7 and drives the pulley 6 or 7; 11, a home position sensor for detecting the sub-scanning position of the carriage 5 held by the CIS 4; 13, a density reference plate which is attached to the end of the home position sensor 11 on the platen glass 1 and serves as a reference for adjustment control of the light quantity and reference density read operation; and 12, an operation unit which is constituted by a switch for operating the image processing apparatus and a display for displaying the state of the image reader. Operation conditions are set and an operation is selected on the basis of an input signal from the operation unit 12.

[0024] The arrangement of the CIS 4 will be described in detail with reference to Fig. 2.

[0025] Reference numeral 4a denotes a line light source unit which is made up of an LED light source unit 4b arranged at the end of the light source unit 4a, and a light guide 4c for uniformly diffusing light from the LED light source unit 4b in the main scanning direction.

[0026] Irradiation light emerging from the light guide 4c is reflected by the document 3 on the platen glass 1. The reflected light forms via a SELFOC lens array 4d an image on a multi-chip sensor 4e which is fixed to a substrate 4f and obtained by arraying a plurality of sensor chips in the main scanning direction.

[0027] The light of the formed image is photoelectrically converted by the multi-chip sensor 4e, and sequentially output as image signals.

[0028] The light intensity of the LED light source unit 4b is controlled by a constant current circuit (to be described in detail later) controllable by a constant current. The ON time of the LED light source unit 4b is controlled by pulse width modulation within the read time of one line of the multi-chip sensor 4e, thereby controlling the light quantity incident on the multi-chip sensor 4e.

[0029] The multi-chip sensor 4e will be explained in detail with reference to Fig. 3.

[0030] In the multi-chip sensor 4e adopted in the first embodiment, about 650 pixels are arrayed in the main scanning direction per sensor chip, and eight sensor

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chips of this type are arrayed in the main scanning direction.

[0031] This arrangement enables reading one line (A4-size, 210 mm-wide document) at a resolution of 600 dpi.

[0032] In order to drive the multi-chip sensor 4e, a driving circuit 21 uses a driving clock pulse for driving the multi-chip sensor 4e so as to read all pixels which constitute one line within a predetermined time, a reset pulse for resetting an output value every pixel in outputting charges from the pixel, and a horizontal sync signal serving as a trigger which starts read of one line.

[0033] Image signals are output from respective pixels in synchronism with the timings of these pulses, and sequentially output via an output circuit 41 having an AGC circuit, A/D conversion circuit, and the like.

[0034] The image processor of the image processing apparatus which performs various image processes for an image signal output from the CIS 4 will be explained with reference to Fig. 4.

[0035] The output circuit 41 comprises an Automatic Gain Controller (AGC) circuit 41a which adjusts the gain of an image signal output from the CIS 4, and an A/D conversion circuit 41b which converts an analog signal into a digital signal.

[0036] Reference numeral 42 denotes an LED control circuit (to be described in detail later) which controls the light quantity of the LED light source unit 4b serving as a light source in the CIS 4. The LED control circuit 42 is constituted by a portion which controls to obtain a predetermined light quantity when the LED light source unit 4b is ON and an image signal is accumulated in the multi-chip sensor 4e, and to keep light sources ON at a predetermined light quantity ratio when light sources of a plurality of colors are ON, and a portion which controls the LED ON timing (PWM (Pulse Width Modulation circuit) control portion which turns on the LED for a predetermined time at a predetermined timing).

[0037] Reference numeral 43 denotes a control circuit which performs image processing for an image signal output from the output circuit 41, and controls the LED control circuit 42.

[0038] The control circuit 43 incorporates an image processing circuit 43a which executes correction such as shading correction and luminance correction for an image signal, an image processing memory 43b, a CPU 43c which controls the overall image processing apparatus, a control memory 43d, an interface circuit 43f, and a motor driving circuit 43e.

[0039] The CPU 43c sets various operation conditions of the image processing apparatus such as the offset value and gain value of the above-described output circuit 41, the PWM control value of the LED of the LED control circuit 42, various parameters for image processing to the image processing circuit 43a, and the interface conditions of the interface circuit 43f. Further, the CPU 43c controls the start and stop of the operation, and controls the interface with an external device.

[0040] The data bus of the CPU 43c allows reading out via the image processing circuit 43a image data which is processed by the image processing circuit 43a and stored in the image memory 43b.

[0041] In reading an image, the CPU 43c detects the reference position of the CIS 4 by using the home position sensor 11. The CPU 43c controls the motor driving circuit 43e and causes the stepping motor 10 to output a predetermined excitation pattern so as to move the CIS 4 at a predetermined speed in the sub-scanning direction in reading an image, thereby a desired image is read.

[0042] Control and operation concerning image reading and image processing of the image processing apparatus in the first embodiment will be described with reference to Figs. 1 to 4.

[0043] In reading a document, start of reading operation is instructed via the operation unit 12. Whether the home position sensor 11 detects the position of the carriage 5 is checked. If the home position sensor 11 does not detect the position, the stepping motor 10 is driven. The motor is stopped at a position after the home position sensor 11 detects the position of the carriage 5 and the motor is further driven for a predetermined number of pulses. Then, the carriage 5 is located at the home position.

[0044] If the home position sensor 11 detects the carriage 5 from the beginning, the stepping motor 10 is driven in the sub-scanning direction. After the carriage 5 passes through the home position sensor 11 once, the stepping motor 10 is rotated in the reverse direction. The stepping motor 10 is stopped at a position after the home position sensor 11 detects the carriage 5 again and the motor 10 is further driven for a predetermined number of pulses. Then, the carriage 5 is located at the home position.

[0045] Before image reading starts, the PWM values for respective colors of the LED light source are set using the above-described density reference plate 13 at this position.

[0046] The PWM values are set by detecting the image signal value of the CIS 4. First, the offset value and gain value of the output circuit 41 are set to predetermined reference values, the light quantity ratio of the respective colors of the LED is set, and then the PWM values of the colors are set.

[0047] Next, the correction value for shading correction is set based on an image signal obtained by irradiating the density reference plate 13 in the set light quantity.

[0048] After the above operation is completed, the stepping motor 10 drives the carriage 5 in the sub-scanning direction to start reading a document image.

[0049] After reading starts, the optical image of a document is photoelectrically converted, and the image signal of the document image is processed.

[0050] The image signal is sampled, and then undergoes signal offset level correction and signal amplifica-

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tion processing in the output circuit 41. After analog signal processing ends, the image signal is converted into a digital signal by the A/D conversion circuit 41b, and the digital signal is output.

[0051] The digital image signal is stored in the image memory 43b after processed with shading correction, spatial filter processing, magnification correction, luminance signal conversion, and binarization processing by the image processing circuit 43a in the control circuit 43. Note that various image processing conditions and operation parameters described above can be set by the CPU 43c in the control circuit 43.

[0052] Image data stored in the image memory 43b is output via the interface circuit 43f in synchronism with a control timing with an external device.

[0053] The LED control method of the LED light source unit 4b will be described with reference to Fig. 5.

[0054] In Fig. 5, reference numeral 43 denotes the control circuit shown in Fig. 4. Of the arrangement shown in Fig. 4, only the CPU 43c and control memory 43d are illustrated. As described above, the control circuit 43 controls the whole image reading apparatus.

[0055] The LED light source unit 4b has a Red LED, Green LED, and Blue LED. The LED control circuit 42 has LED driving units 42a, 42b, and 42c each including a constant current circuit and switching circuit in correspondence with each LED of the LED light source unit 4b. The LED driving units 42a, 42b, and 42c are independently connected to respective color LEDs (red, green, and blue).

[0056] All the LEDs receive a common potential. The constant current values of the constant current circuits, and switch-on times (ON times) in the LED driving units 42a, 42b, and 42c can be changed by control signals based on image signals input from the multi-chip sensor 4e to the control circuit 43.

[0057] Initial values in the control circuit 43 and the LED ON ratio can be set using the operation unit 12.

[0058] To make the explanation clear, the first embodiment is based on the following premise. However, this premise does not limit the present invention.

[0059] The LED light source unit 4b is an LED light source (array type and light guide type) having R, G, and B (Red, Green, and Blue) wavelengths.

[0060] Light-receiving amounts pix_R, pix_G, and pix_B of the multi-chip sensor 4e are proportional to LED light quantities I_R, I_G, and I_B. Since the light quantities are the products of light intensities (I_R, I_G, and I_B) and irradiation times (t_R, t_G, and t_B),

$$pix_R \propto I_R = I_R \times t_R$$

$$pix_G \propto I_G = i_G \times t_G$$

$$pix_B \propto I_B = I_B \times t_B$$

hold. Constant current values which determine the light intensities of the respective LEDs and the ON times of the LEDs are independently stored. The LEDs are independently turned on and driven based on these values, and can emit desired light quantities. When the LED light source unit 4b is turned on and image signals are accumulated in the multi-chip sensor 4e, the light source can be turned on so as to obtain a predetermined light quality. When light sources of a plurality of colors are turned on, they can be turned on at a predetermined light quantity ratio.

[0061] A portion which controls the LED ON timing is a pulse width modulation (PWM) control portion which turns on the LED for a predetermined time with reference to a predetermined timing.

[0062] An image output signal value output from the A/D conversion circuit 41b is an 8-bit 256-level output using the output value of a white reference plate as 255 and the output value of a black reference plate (or light-off state) as 0.

[0063] The control circuit 43 performs software control mainly using the CPU 43c. However, control of the present invention may be realized by using hardware mainly using a gate array.

[0064] The detailed arrangement and operation of the image processing circuit 43a will be described.

[0065] The arrangement will be first explained.

[0066] As shown in Fig. 6, the image processing circuit 43a is constituted by a shading correction block 61a, a filter block 62a, a magnification correction block 63a, a luminance signal conversion block 64a, a binarization processing block 65a, and memories 61b, 62b, 63b, 64b, and 65b which correspond to the respective blocks and store image data, coefficients, and the like. Instead of arranging the memories 61b, 62b, 63b, 64b, and 65b in the image processing circuit 43a, the memory 43b can, for example, be utilized. In this case, memory capacities necessary for the blocks 61a to 65a are ensured in the memory 43b in advance.

[0067] The memory 61b of the shading correction block 61a, the memory 63b of the magnification correction block 63a, and the memory 64b of the luminance signal conversion block 64a allow writing image data, reading out and writing data from the CPU 43c of the control circuit 43.

[0068] Fig. 7 is a block diagram showing the detailed arrangement of the luminance signal conversion block 64a in Fig. 6, and specifically shows a circuit block for converting input image luminance data of one pixel into corresponding density data.

[0069] The memory 64b has three correction table memories 74a, 74b, and 74c for different sensor chip characteristics. The luminance signal conversion block 64a comprises an address counter 71 for counting the number of pixels, a selector 73 for switching and controlling accesses to the table memories 74a, 74b, and 74c in accordance with the address counter value, and a setting register 72 for holding a comparison value to

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be compared with an output value from the address counter 71 and selection settings for the selector 73.

[0070] Luminance signal conversion operation will be explained.

[0071] Fig. 8 shows the structure of the density reference plate 13. The density reference plate 13 is made up of two reference density areas: a white reference area 13a used for shading correction in reading an image and a halftone gray reference area 13b used to determine sensor chip characteristics.

[0072] Setting of a correction table corresponding to a sensor chip will be explained with reference to the flow chart of Fig. 25. As described above, the white reference plate area 13a is read by the multi-chip sensor 4e to obtain shading correction data, and shading correction is done based on this data.

[0073] Thereafter, the halftone gray reference area 13b is read by the multi-chip sensor 4e (step S101), and the read image data is stored in the memory 63b of the magnification correction block 63a.

[0074] The CPU 43c in the control circuit 43 reads out image data stored in the memory 63b, and calculates the average of pixel data at a halftone density for each sensor chip (step S102). The calculated average data is stored in the memory 43d. The halftone gray reference value stored in the memory 43d is compared with the average of each sensor chip, and which of conversion data in the correction table memories 74a, 74b, and 74c is to be used is set for each memory chip (steps S013 to S107).

[0075] The multi-chip sensor 4e adopted in the first embodiment is made up of eight sensor chips, as shown in Fig. 3. Which of correction tables in the three correction table memories 74a, 74b, and 74c is to be used as a correction table for each of the eight sensor chips is set in the setting register 72 (step S108).

[0076] Figs. 9A to 9C show examples of the correction characteristic of the correction table. Fig. 9B shows a table (correction table 2) whose correction characteristic is almost ideal. Fig. 9A shows a characteristic table (correction table 1) whose halftone image data is smaller than a reference value. Fig. 9C shows a characteristic table (correction table 3) whose halftone image data is larger than the reference value.

[0077] For example, if the halftone average of the first sensor chip is almost equal to the above-mentioned reference value in the memory (YES in step S103), correction table 2 is set (step S104). If the halftone average of the second sensor chip is larger than the above-mentioned reference value in the memory (YES in step S105), correction table 3 is set (step S106). If the halftone average of the third sensor chip is smaller than the above-mentioned reference value in the memory (NO in step S105), correction table 1 is set (step S107). In this way, which of correction tables stored in the three correction table memories 74a, 74b, and 74c is to be used as correction table data corresponding to each of the eight sensor chips is set. The setting information is stored in the setting register 72 of Fig. 7 (step S108). This operation is executed for all the sensor chips (step S109).

[0078] When the characteristic of the sensor chip is known in advance, a correction table may be selected and set for each sensor chip by using the operation unit 12.

[0079] In the first embodiment, a correction table is not set for each sensor chip, but a smaller number of correction tables than the number of sensor chips is set, as described above. Then, a plurality of sensor chips share the correction tables, which can prevent increasing the size of the image processing circuit 43a even with many sensor chips.

[0080] However, the first embodiment is not limited to the above arrangement, and a correction table may be set for each sensor chip.

[0081] As the power consumption of the image processing apparatus is reduced, degradation in the image quality of a halftone image cannot be prevented by only shading correction. In this case, the arrangement according to the first embodiment is very effective.

[0082] The flow of an operation of the image processing circuit will be explained with reference to Figs. 4, 6, and 26.

[0083] As described above, an image signal from the multi-chip sensor 4e that is converted into a digital signal by the A/D conversion circuit 41b is input to the image processing circuit 43a (step S120). The image signal undergoes shading correction in the shading correction block 61a, and edge emphasis processing or smoothing processing in the filter block 62a. Further, the image signal undergoes reduction/enlargement processing in the image magnification correction block 63a, and is input to the luminance signal conversion block 64a.

[0084] In the first embodiment, image data is processed as 8-bit data, and image data of one line are sequentially processed in synchronism with a horizontal sync signal.

[0085] Image data of one line are input to the luminance signal conversion block 64a in an order of pixels from one side of the eight sensor chips. At this time, the number of pixels is counted by the address counter 71. Written in the setting register 72 is the number of a correction table memory to be selected (step S122) when the address value of the first pixel of each sensor chip coincides with a setting value set in the setting register 72 (step S121).

[0086] For example, if the first chip of the multi-chip sensor corresponds to setting of correction table memory 1, all the image signals from the first chip are corrected in accordance with correction table 1 of correction table memory 1 (74a) (step S123). If the count value of the address counter 71 coincides with the first address of the second chip and this count value is set to selection of correction table 2, all the image signals from the second chip are corrected in accordance with correction table 2 of correction table memory 2 (74b) (step

S123). This operation is repeated until all the image signals are processed (step S124).

[0087] In this fashion, image signals from the 8-chip sensor are corrected based on characteristics which are suitable for respective chip characteristics. Therefore, image data can be corrected even at the halftone portion of an image with less density nonuniformity caused by the characteristic difference between chips.

[0088] In the first embodiment, a case in which the multi-chip sensor 4e is formed from eight chips is explained. However, the number of chips is a design rule, and an arbitrary number of chips can be connected.

[0089] Further, the number of correction tables is three in the first embodiment, but is not limited to this, and an arbitrary number of correction tables can be set. Also in this case, a correction table to be used may be set in accordance with the intermediate value of the signal value of the halftone gray reference area 13b output from each sensor chip.

[0090] The first embodiment has exemplified the use of the CIS, but is not limited to this. For example, the linearity correction method of the first embodiment can be preferably applied in the use of a CCD or MOS type image sensing element which is divided into a plurality of areas and reads out signals from the respective areas via different output systems.

(Second Embodiment)

[0091] Fig. 10 is a block diagram showing an image processing apparatus according to the second embodiment of the present invention.

[0092] Reference numeral 202 denotes a contact image sensor (CIS) module having a multi-chip sensor functioning as an image sensing unit which includes a plurality of pixels and a plurality of output units for outputting signals from the pixels. In a multi-chip sensor 2024, as shown in Fig. 11, a plurality of sensor chips (chip1 to chip16 in Fig. 11) on each of which a plurality of pixels are arrayed in one direction (main scanning direction) are arrayed on a mounting substrate 2025 in the same direction as that of the pixel array.

[0093] The arrangement of the CIS module 202 in the second embodiment will be described.

[0094] In the CIS module 202, as shown in Fig. 12, a cover glass 2021, an illumination light source 2022 formed from an LED, a ×1 imaging lens 2023, such as a SELFOC lens, and the multi-chip sensor 2024 are mounted on the, substrate 2025. These parts are attached to a mold 2026 to form the integral CIS module 202.

[0095] Fig. 13 is a perspective view showing the CIS module 202 of Fig. 12. The same reference numerals as in Fig. 12 denote the same parts.

[0096] Fig. 14 shows details of one sensor chip (e.g., chip1) of the multi-chip sensor 2024.

[0097] In Fig. 14, each rectangle represents a reading pixel. For a 600-dpi ×1 reading multi-chip sensor, the pixel interval is 42 × 42 μm. Reference numeral 2024-1 denotes a pixel array for reading red (R) light; and 2024-2 and 2024-3, pixel arrays for reading green (G) light and blue (B) light, respectively.

[0098] Each pixel on the pixel array 2024-1 is covered with an R color filter; each pixel on the pixel array 2024-2, with a G color filter; and each pixel on the pixel array 2024-3, with a B color filter. A photodiode as a photoelectric converter is formed below each color filter. As described above, for 600 dpi, the three pixel arrays are formed at a pixel interval of 42 μm in the sub-scanning direction (direction in which a document or the multi-chip sensor 2024 moves). The pixel pitch in the main scanning direction is also 42 μm.

[0099] The photodiode generates charges corresponding to an incident light quantity during the accumulation time.

[0100] The three pixel arrays having different optical characteristics form a monolithic structure on a single silicon chip so as to arrange the pixel arrays parallel to each other in order to read the same line of a document by the R, G, and B pixel arrays.

[0101] Reference numeral 2024-4 denotes a CCD shift register serving as a charge transfer unit. By applying shift pulses to pixels at the first timing of one line, charges move from the pixels of the pixel arrays 2024-1, 2024-2, and 2024-3 to the charge transfer unit 2024-4.

[0102] By applying a transfer clock to the charge transfer unit 2024-4, charges which have moved to the charge transfer unit 2024-4 are transferred in time division to an output amplifier unit 2024-5 in an order of G, B, R, G, B, R,.... The output amplifier unit 2024-5 converts the charges into voltages, and sequentially outputs signals as voltage outputs in an order of G, B, R, G, B, R,....

[0103] An analog signal processor 101 in Fig. 10 comprises a gain offset adjustment circuit which adjusts the gain offsets of signals from respective output units (OS1 to OS16), and an A/D converter which converts an analog signal into a digital signal.

[0104] The analog signal processor 101 has two analog processors (AP1 and AP2). Each analog processor receives analog signals via eight channels, multiplexes the signals, and outputs a digital signal via one channel in time division.

[0105] A sorting unit 102 converts input digital signals into appropriately sorted R, G, and B digital signals. First, signals from an R pixel array, signals from a G pixel array, and signals from a B pixel array on chip1 are output in parallel pixel by pixel until signals of all the pixels on chip1 is read out. Then, signals from an R pixel array, signals from a G pixel array, and signals from a B pixel array on chip2 are output in parallel pixel by pixel. In this manner, color signals are sequentially output in parallel from every sensor chip.

[0106] A shading correction unit 103 performs shading correction for each color. The shading correction unit 103 has shading correction circuits for the respective

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colors (103r, 103g, and 103b).

[0107] A CPU 108 controls the entire image processing apparatus.

[0108] A linearity correction unit 104 is a characteristic feature of the second embodiment, and performs linearity correction for digital signals having undergone shading correction by sensor chip and color, i.e., for a plurality of image signals having different linearity characteristics. The second embodiment adopts (a total of three) linearity correction circuits (104a to 104c) for the respective colors.

[0109] The above arrangement is the best in consideration of the balance between the circuit scale and the processing speed. However, the present invention is not limited to this arrangement, and linearity correction circuits may be arranged for respective sensor chips (i.e., 16 linearity correction circuits are prepared), or linearity correction circuits may be arranged for respective sensor chips and colors (i.e., 48 linearity correction circuits are prepared). Such an arrangement does not require the following main scanning position determination unit.

[0110] For a monochrome image, one linearity correction circuit is desirably arranged as a whole in consideration of the balance between the circuit scale and the processing speed. However, a linearity correction circuit may be arranged for each sensor chip.

[0111] Figs. 15A and 15B are a graph and table for explaining the concept of linearity correction.

[0112] An input signal is represented by an x-coordinate, and a corresponding output signal is represented by a y-coordinate. In Fig. 15A, the x-axis is divided into four domains of definition. For a 10-bit input signal, X takes a value of 0 to 1023.

[0113] A linear function is defined as follows for each domain of definition.

$$0 \leqq X < x1: Y = A1*X + B1;$$

$$x1 \leqq X < x2: Y = A2*X + B2;$$

$$x2 \leqq X < x3: Y = A3*X + B3;$$

$$x3 \leqq X < x4: Y = A4*X + B4;$$

where X is an input signal, Y is an output signal, A1 to A4 are multiplicative coefficients, and B1 to B4 are additive factors of the y-intercept of the linear function. Each linear function can be expressed by a straight line, but is a line segment because the domain of definition is determined. The CPU 108 sets respective line segments to be continuous. These settings are shown in the table of Fig. 15B.

[0114] As a result, a line graph which passes through coordinates (0,0) and (1023,1023), slightly projects upward, and is broken at three points is realized as shown in the graph of Fig. 15A.

[0115] Setting the linearity correction function enables linearity correction. A curved graph can achieve more appropriate correction than a line graph. However, the deviation from the ideal straight line of the linearity of each signal is not large in actual measurement, and is about 8 levels at the center for 10 bits or 2 levels for 8 bits. The linearity can be satisfactorily corrected by a line graph.

[0116] In order to correct the linearity by a four-segment-line graph, the domain of definition is divided into four. In the arrangement of the second embodiment, a line graph having an arbitrary number of line segments can also be realized by continuously connecting the line segments.

[0117] A method of obtaining the linearity correction function as shown in Figs. 15A and 15B will be explained with reference to the flow chart of Fig. 27.

[0118] In linearity correction, a halftone chart is read by the CIS module 202 in order to obtain halftone correction data (step S201). First, a chart with a density D of 0.3 is prepared and read, shading correction (to be described later) is performed, and a chart reading level is attained for each color of each of 16 chips. Then, the level averages of all the 16 chips are obtained for respective R, G, and B colors. The obtained averages are defined as the target values of the respective colors, and made to correspond to signal levels in the CPU 108 such that the obtained target values are output in response to the signal levels of the respective chips when the D=0.3 chart is read.

[0119] To correct a dark portion, a chart with a density D of 1.1 is prepared, shading correction is performed, and a chart reading level is attained for each color of each of 16 chips. The level averages of all the 16 chips are obtained for respective R, G, and B colors. The obtained averages are defined as the target values of the respective colors, and made to correspond to signal levels in the CPU 108 such that the obtained target values are output in response to the signal levels of the respective chips when the D=1.1 chart is read.

[0120] To correct a bright portion, a chart with a density D of 0.2 is prepared, shading correction is performed, and a chart reading level is attained for each color of each of 16 chips. The level averages of all the 16 chips are obtained for respective R, G, and B colors. The obtained averages are defined as the target values of the respective colors, and made to correspond to signal levels in the CPU 108 such that the obtained target values are output in response to the signal levels of the respective chips when the D=0.2 chart is read.

[0121] As a result, input and output values are attained for the black level, D=1.1, D=0.3, D=0.2, and white level. Coefficients (An and Bn) representing a linearity correction function which expresses a line segment between input and output values are calculated based on the input and output values. These correction

EP 1 289 265 A2

coefficients are obtained for each color of each chip (step S202). The calculated correction coefficients are stored in correspondence with each sensor chip (step S203). In this manner, correction coefficients for all the sensor chips are calculated and stored (step S204). The use of this function enables correcting the linearity so as to make the reading levels of the chips approach each other.

[0122] The operation of obtaining the linearity correction function may be done in shipping from a factory (after shipping, the same value is used), or every document reading operation.

[0123] Fig. 16 is a block diagram showing details of the linearity correction unit 104. Fig. 16 shows one (for R) of the linearity correction circuits 104a to 104c. The remaining linearity correction circuits also have the same arrangement.

[0124] An x-axis section determination unit 1041 checks a section along the x-axis in Figs. 15A and 15B, and determines which of four linear functions corresponds to this section. A determination output is given by n (section determination signal), and sent to a coefficient selection unit 1042. A main scanning position determination unit 1045 outputs a main scanning position signal k representing which of sensor chips arrayed in the main scanning direction outputs a signal to be processed. A delay unit 1043 adjusts the clock phase.

[0125] The coefficient selection unit 1042 selects a multiplicative coefficient Akn and additive factor Bkn on the basis of the section determination signal n and main scanning position signal k, and sends the multiplicative coefficient Akn and additive factor Bkn to a multiplication circuit 1044 and addition circuit 1045, respectively. As a result,

$$Y = Akn*X + Bkn$$

is solved, and linearity correction described with reference to Figs. 15A and 15B is realized for each chip.

[0126] The coefficients Akn and Bkn in the second embodiment change depending on the signal level of a signal to be corrected and a sensor chip which outputs the signal to be corrected. One linearity correction circuit has 64 (= × 4 x-axis sections × 16 sensor chips) different coefficients.

[0127] The coefficient selection unit 1042 in the second embodiment has 64 registers formed from flip-flops for the multiplication circuit 1044 in one linearity correction circuit, and 64 registers formed from flip-flops for the addition circuit 1045. Each register outputs a coefficient. Each register receives a proper value from the CPU in power-on operation. The coefficients Akn and Bkn are given as register setting values, which greatly shortens the write time in comparison with write of all input and output values which represent curves in the LUT.

[0128] The present invention is not limited to the above arrangement, and each coefficient value may be stored in, e.g., a ROM or SRAM. However, the data amount of coefficients is not so large, and storing the coefficients in the ROM or SRAM wastes many addresses and increases the cost. For this reason, the use of registers is the most preferable in consideration of the space and cost.

[0129] As described above, the linearities of image signals output from sensor chips having different linearities can be made to approach each other, thereby reducing the difference in reading halftone density.

[0130] A clock generator 121 generates a clock VCLK every pixel. A main scanning address counter 122 counts clocks from the clock generator 121, and generates a 1-line pixel address output. A decoder 123 decodes a main scanning address from the main scanning address counter 122, and generates line sensor driving signals (not shown) such as a shift pulse (ϕSH) and reset pulse (ϕR), and a line sync signal HSYNC. The main scanning address counter 122 is cleared in synchronism with a HSYNC signal, and starts counting of the main scanning address of the next line.

[0131] The operation of the image processing apparatus shown in Fig. 10 will be explained with reference to the flow chart of Fig. 28.

[0132] The multi-chip sensor 2024 outputs an analog signal (step S210). Fig. 17 is a timing chart for explaining the timing of a driving signal to the multi-chip sensor 2024 and the timing of an analog signal output from the multi-chip sensor 2024.

[0133] The timings in this timing chart are the same in all sensor chips. ϕSH represents a line sync signal, which also serves as a charge transfer pulse from the photodiode of each pixel to the charge transfer unit 2024 4 (Fig. 14). As shown in Fig. 17, transferred charges are sequentially output from the output amplifiers OS1 to OS18 in an order of G1, B1, R1, G2, B2, R2, ... ϕRS represents a reset pulse, which supplies a reset signal to the multi-chip sensor 2024.

[0134] An analog signal output from the CIS module 202 is input to the analog signal processor 101, undergoes gain adjustment and offset adjustment, and is A/D-converted. The sorting unit 102 properly sorts signals, and converts them into, e.g., 10-bit digital image signals R1, G1, and B1 for respective color signals.

[0135] The image signals are input to the shading correction unit 103, and undergo shading correction for the respective colors by using signals obtained by reading a white reference plate (not shown).

[0136] Details of shading correction operation will be described with reference to Fig. 18. For illustrative convenience, Fig. 18 shows only one (103r in Fig. 18) of the shading correction circuits 103r, 103g, and 103b included in the shading correction unit 103.

[0137] In shading data acquisition operation, the light source is turned off, and black reference data Bk(i) is sampled for each pixel and stored in line memory 1. The CIS module 202 is moved to the position of a white ref-

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erence plate. the light source is turned on, and white reference data WH(i) is sampled and stored. Calculation of converting the data into white shading correction data

$$1/(WH(i) - Bk(i))$$

is executed, and the resultant data is stored in line memory 2.

[0138] In actual image reading, calculation: OUT(i) = (IN(i) - Bk(i)) × 1/(WH(i) - Bk(i)) is performed in real time for each pixel, and data having undergone shading correction is output.

[0139] In this case, IN(i) represents the ith input data; OUT(i), the ith output data; Bk(i). the ith black reference data in line memory 1; and 1/(WH(i) - Bk(i)), the ith white shading correction data.

[0140] In general, the CIS desirably has a memory which stores the correction value of each pixel even for black shading because black noise is large due to a large pixel and the offset value is different between a plurality of chips. To the contrary, the CCD generally has a uniformly subtracting register.

[0141] For cost priority, the CIS can also take an arrangement which reduces the cost by using the black correction value of each chip or the like.

[0142] Fig. 19 is a view for explaining the timing of a sorted signal output from the sorting unit 102. Fig. 19 shows the timing of only one of R, G, and B colors for illustrative convenience.

[0143] A sensor-specific dummy signal is output for a while after the line sync signal HSYNC. In an effective pixel area, n sensor chip signals are sequentially output in an order of Chip1, Chip2,..., ChipN from the first chip. In the second embodiment, N = 16. Since each chip has 468 pixels, 468 × 16 = 7488 effective pixels are obtained. Then, a dummy pixel signal is output again. While signals are output from respective chips, the linearity correction circuits 104a, 104b, and 104c output corresponding main scanning position signals k from their main scanning position determination units 1046 shown in Fig. 16.

[0144] Signals from the shading correction unit 103 are input to the linearity correction unit 104, and undergo linearity correction by the above-described method.

[0145] First, signals from the shading correction unit 103 are input parallel to each other to the delay units 1043 and x-axis section determination units 1041 of the linearity correction circuits 104a, 104b, and 104c. Then, each x-axis section determination unit 1041 determines the signal level of the signal (section described with reference to Figs. 15A and 15B), and outputs a corresponding section determination signal n (step S211).

[0146] The main scanning position determination unit 1046 outputs a main scanning position signal k representing which of sensor chips outputs the signal input from the shading correction unit 103 (step S212).

[0147] The coefficient selection unit 1042 outputs coefficients Akn and Bkn selected in accordance with the section determination signal n and main scanning position signal k (step S213). The multiplication circuit 1044 multiplies the signal from the delay unit 1043 by the coefficient Akn. The addition circuit 1045 adds the signal from the multiplication circuit 1044 and the coefficient Bkn (step S214).

[0148] A signal from the linearity correction unit 104 is input to an image processing circuit (not shown), and undergoes various correction processes such as color correction and gamma correction. The above processing is performed for all image data (step S215).

[0149] An image forming apparatus in which the above-described image processing apparatus is mounted will be explained.

[0150] In Fig. 20, reference numeral 200 denotes an image scanner section which reads a document and executes digital signal processing; and 300, a printer section which prints out, on a sheet in full colors, an image corresponding to the document image read by the image scanner section 200.

[0151] In the image scanner section 200, a document 204-1 set on a platen glass 205 by the platen cover of an automatic document feeder (ADF) 203 is irradiated with light from the illumination light source 2022 in the CIS module 202 having the arrangement shown in Fig. 12. Light reflected by the document 204-1 forms an image on the multi-chip sensor 2024 via the lens 2023.

[0152] Alternatively, the CIS module 202 is stopped at the position of a flow scanning glass 208, and a document is read at this position. In this operation, document sheets are successively supplied from the ADF 203 and read.

[0153] The multi-chip sensor 2024 separates optical information from the document into colors, reads R (Red), G (Green), and B (Blue) components of the full-color information, and sends the components to a signal processor 100 in Fig. 10. Each of the pixel arrays 2024-1 to 2024-3 for respective colors of the multi-chip sensor 2024 is made up of, e.g., 7,500 pixels. Thus, an A3-size document 297 mm in the widthwise direction, which has the maximum size among documents set on the platen glass 205, can be read at a resolution of 600 dpi.

[0154] To read the document 204-1 on the platen glass 205, the CIS module 202 is mechanically moved at a velocity V in the sub-scanning direction to scan the entire surface of the document 204-1.

[0155] A white reference plate 206 is used to obtain white correction data for data read by the R, G, and B pixel arrays 2024-1 to 2024-3 of the multi-chip sensor 2024. The white reference plate 206 exhibits an almost uniform reflection characteristic for visible light, and has a visually white color. By using data obtained by reading the white reference plate 206, data output from the R, G, and B pixel arrays 2024-1 to 2024-3 are corrected.

[0156] On the stage subsequent to the signal processor 100, a read signal is electrically processed and sep-

arated into M (Magenta), C (Cyan), Y (Yellow), and Bk (Black) components, and these components are sent to the printer section 300. One of the M, C, Y, and Bk components is sent to the printer section 300 every document scanning in the image scanner section 200, completing a copy printout.

[0157] In the printer section 300, M, C, Y, and Bk image signals are sent to a laser driver 312. The laser driver 312 modulates and drives a semiconductor laser 313 in accordance with the image signal. A laser beam scans a photosensitive drum 317 via a polygon mirror 314, f-θ lens 315, and mirror 316.

[0158] The developing unit is constituted by a magenta developing unit 319, cyan developing unit 320, yellow developing unit 321, and black developing unit 322. The four developing units alternately come into contact with the electrostatic drum 317, and develop M, C, Y, and Bk electrostatic latent images formed on the electrostatic drum 317 with corresponding toners. A sheet fed from a sheet cassette 324 or 325 is wound around a transfer drum 323, and a toner image developed on the electrostatic drum 317 is transferred to the sheet.

[0159] After toner images of four, M, C, Y, and Bk colors are sequentially transferred, the sheet is discharged via a fixing unit 326.

[0160] Note that the image reader with a CIS and the image processing apparatus described in the first embodiment can also be applied to the image scanner section 200 of Fig. 20.

(Third Embodiment)

[0161] The third embodiment will be explained. Only the difference from the second embodiment will be described, and a description of the same part will be omitted.

[0162] Fig. 21 is a block diagram showing an image processing apparatus according to the third embodiment of the present invention.

[0163] Reference numeral 213 denotes a center-division two-end-read type CCD image sensor serving as an image sensing unit which includes a plurality of pixels and a plurality of output units for outputting signals from the pixels.

[0164] Fig. 22 is a block diagram for explaining details of the CCD image sensor 213.

[0165] Reference symbols P1, P2,..., P7500 denote photodiodes as photoelectric converters which read and accumulate image information for 7,500 pixels in the main scanning direction. The sensor is divided into left and right parts at the boundary between the 3750th and 3751st central pixels. Charges in the photodiodes are transferred to CCD analog shift registers 2131, 2133, 2135, and 2137 in response to shift pulses (not shown).

[0166] More specifically, charges in odd-numbered pixels P1 to P3749 are transferred to the CCD analog shift register 2131, and output as OS1 from an output buffer 2132 in response to a transfer clock.

[0167] Charges in even-numbered pixels P2 to P3750 are transferred to the CCD analog shift register 2133, and output as OS2 from an output buffer 2134 in response to a transfer clock.

[0168] Charges in odd-numbered pixels P3751 to P7499 are transferred to the CCD analog shift register 2135, and output as OS3 from an output buffer 2136 in response to a transfer clock.

[0169] Charges in even-numbered pixels P3752 to P7500 are transferred to the CCD analog shift register 2137, and output as OS4 from an output buffer 2138 in response to a transfer clock.

[0170] In this fashion, signals from monochrome 7,500 pixels are divided into left and right parts, further divided into odd and even numbers, and read out as four output signals. For this reason, OS1 to OS4 vary in linearity, similar to the second embodiment. Since the sensor is divided at the center, the halftone reading density becomes different between the left and right sides at boundary of the division line, degrading the image quality.

[0171] The third embodiment will exemplify a monochrome image. For a color image, R, G, and B filters are formed on photodiodes, and three CCD image sensors are arranged parallel to each other.

[0172] The analog signals OS1 to OS4 output from the CCD image sensor 213 undergo gain & offset adjustment by an analog processor 151. Then, the signals OS1 to OS4 are A/D-converted, and output as two digital signals DS1 and DS2. A sorting unit 152 corrects a state in which the image reading directions of DS1 and DS2 are opposite by 180°, and sorts signals so as to appropriately connect signals from the 3750th and 3751st central pixels. A signal R1 is a sorted signal. A shading unit 153 performs the same shading correction as that in the first embodiment.

[0173] A linearity correction unit 154 executes the same linearity correction as that described in the second embodiment with reference to Figs. 15A, 15B, and 16.

[0174] Fig. 21 shows an arrangement for a monochrome signal. For a color signal, red, green, and blue shading correction circuits and linearity correction circuits are arranged parallel to each other.

[0175] Fig. 23 is a timing chart for explaining an image signal after the sorting unit 152. Reference symbol HSYNC denotes a line sync signal; and P1 to P7500, image signals which are so sorted as to make the central image signals P3750 and P3751 adjacent to each other. A main scanning position signal k is generated in correspondence with each pixel. k = 1 is generated for the odd-numbered pixels P1 to P3749; k = 2, for the even-numbered pixels P2 to P3750; k = 3, for the odd-numbered pixels P3751 to P7499; and k = 4, for the even-numbered pixels P3752 to P7500.

[0176] The main scanning position signal k = 1 to 4 is generated by a main scanning position determination unit 1048 in Fig. 16.

[0177] Similar to the second embodiment, the ar-

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rangement of the linearity correction unit 154 in Fig. 16 and linearity correction in Figs. 15A and 15B realized by the linearity correction unit 154 can suppress the reading density difference between right and left pixels classified at the center and between odd- and even-numbered pixels, thereby improving the image quality.

[0178] Linearity correction in the third embodiment is not limited to the method of the second embodiment, but can also be achieved by the method described in the first embodiment.

[0179] Fig. 24 is a schematic view showing the sectional arrangement of an image forming apparatus in which the above-described image processing apparatus is mounted. In Fig. 24, the same reference numerals as in Fig. 20 denote the same parts, and a description thereof will be omitted. Reference numeral 200 denotes an image scanner section which reads a document and executes digital signal processing; and 300, a printer section which prints out, on a sheet in full colors, an image corresponding to the document image read by the image scanner section 200.

[0180] A light source 209 is formed from a xenon lamp, and illuminates a document. A first mirror 210 deflects optical information of an illuminated document by 90° toward a second mirror 211. The second mirror 211 is formed from a set of two mirrors, and deflects the optical information by 180° to a reduction imaging lens 212. The lens 212 forms the image of the optical information on a CCD image sensor 213. A set of the first mirror 210 and light source 209 scan the document at a velocity V, whereas the second mirror 211 moves at half the velocity in the same direction.

<Other Embodiment>

[0181] The present invention can be applied to a system constituted by a plurality of devices or to an apparatus comprising a single device.

[0182] Further, the object of the present invention can also be achieved by providing a storage medium storing program codes for performing the aforesaid processes to a computer system or apparatus (e.g., a personal computer), reading the program codes, by a CPU or MPU of the computer system or apparatus, from the storage medium, then executing the program.

[0183] In this case, the program codes read from the storage medium realize the functions according to the embodiments, and the storage medium storing the program codes constitutes the invention.

[0184] Further, the storage medium, such as a floppy disk, a hard disk, an optical disk, a magneto-optical disk, CD-ROM, CD-R, a magnetic tape, a non-volatile type memory card, and ROM, and computer network, such as LAN (local area network) and LAN, can be used for providing the program codes.

[0185] Furthermore, besides aforesaid functions according to the above embodiments are realized by executing the program codes which are read by a computer, the present invention includes a case where an OS (operating system) or the like working on the computer performs a part or entire processes in accordance with designations of the program codes and realizes functions according to the above embodiments.

[0186] Furthermore, the present invention also includes a case where, after the program codes read from the storage medium are written in a function expansion card which is inserted into the computer or in a memory provided in a function expansion unit which is connected to the computer, CPU or the like contained in the function expansion card or unit performs a part or entire process in accordance with designations of the program codes and realizes functions of the above embodiments.

[0187] In a case where the present invention is applied to the aforesaid storage medium, the storage medium stores program codes corresponding to the flowcharts shown in Figs. 25 and 26, or 27 and 28 described in the embodiments.

[0188] The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore to apprise the public of the scope of the present invention, the following claims are made.

[0189] An image processing apparatus includes an image sensor formed from a plurality of areas each including a plurality of pixels, and a corrector adapted to correct signals from the plurality of areas of the image sensor. The corrector has a plurality of correction data smaller in number than the areas, and performs correction by selectively using the correction data for each area of the image sensor.

Claims

1. An image processing apparatus **characterized by** comprising:

   an image sensor (4) formed from a plurality of areas each including a plurality of pixels; and a corrector (43a) adapted to correct signals output from the plurality of areas of said image sensor,

   wherein said corrector has a plurality of correction data (74a - 74c) smaller in number than the areas, and performs correction by selectively using any one of the plurality of correction data for each area of said image sensor.

2. The apparatus according to claim 1 further comprises at least one density reference member (13) for detecting characteristics of the plurality of areas of said image sensor (4),

   wherein said corrector (43a) has a setting unit

(72) which sets correction data for each area of said image sensor from the plurality of correction data (74a - 74c) on the basis of a signal obtained by reading said density reference member by said image sensor.

3. The apparatus according to claim 2, **characterized in that** said density reference member (13) has a halftone gray reference area (13b).

4. An image processing apparatus **characterized by** comprising:

an image sensor (4) formed from a plurality of areas each including a plurality of pixels;
a corrector (43a) adapted to correct signals from the plurality of areas of said image sensor; and
a density reference member (13) having a white reference area (13a) and a halftone gray reference area (13b),

wherein said corrector has a plurality of correction data smaller in number than the areas of a sensor chip, and executes first correction (61a) of performing shading correction on the basis of a signal obtained by reading the white reference area by said image sensor, and second correction (64a) of performing correction by selectively using the correction data for each area of said image sensor on the basis of a signal obtained by reading the halftone gray reference area by said image sensor.

5. The apparatus according to claim 4, **characterized in that** said corrector (43a) performs the second correction (54a) after the first correction (51a).

6. The apparatus according to any one of claims 1 to 5, **characterized in that** said corrector (43a) uses common correction data for a signal from said image sensor (4).

7. The apparatus according to any one of claims 1 to 6, **characterized by** further comprising a light source (4a) which irradiates an object to be sensed, and a lens (4d) which forms light from the object into an image on the plurality of areas of said image sensor (4).

8. The apparatus according to any one of claims 1 to 7, **characterized in that** each area of said image sensor is formed from a sensor chip.

9. The apparatus according to any one of claims 1 to 7, **characterized in that** signals from the plurality of areas of said image sensor are output via different output systems.

10. The apparatus according to claim 3 or 4, **characterized in that** the plurality of correction data have correction data for when a signal obtained by reading the halftone gray reference area by each of the plurality of areas represents a substantially predetermined value, correction data for when the signal is larger than the predetermined value, and correction data for when the signal is smaller than the predetermined value.

11. An image processing apparatus **characterized by** comprising:

an image sensor (202, 213) formed from a plurality of areas each including a plurality of pixels; and
a corrector (104, 154) adapted to correct linearity of signals output from the plurality of areas,

wherein said corrector includes:

a multiplier (1044) which multiplies the signals output from the plurality of areas by a coefficient; and
an adder (1045) which adds a coefficient to the signals output from the plurality of areas.

12. The apparatus according to claim 11, **characterized in that**

said corrector (104, 154) comprises a coefficient selector (1042) which selectively outputs a plurality of coefficients, and a first determination unit (1041) which determines signal levels of signals from a plurality of output units, and

said coefficient selector selects a coefficient in accordance with a determination result of said first determination unit.

13. The apparatus according to claim 12, **characterized in that**

said corrector (104, 154) is commonly arranged for signals output from the plurality of output units, and comprises a second determination unit (1046) which determines which of the plurality of output units outputs a signal, and

said coefficient selector (1042) selects a coefficient in accordance with a determination result of said first determination unit (1041) and a determination result of said second determination unit.

14. The apparatus according to any one of claims 11 to 13, **characterized in that**

the apparatus further comprises a sorter (102, 152) which sorts signals output from the plurality of areas so as to sequentially output the signals in an order of a pixel array, and

said corrector (104, 154) receives a signal

3000ID: <EP_____1289265A2_I_>

from said sorter.

15. The apparatus according to any one of claims 11 to 14, **characterized in that**
each area of said image sensor (202, 213) has a plurality of pixel arrays which obtain different pieces of color information, and
said corrector (104, 154) is arranged for each color.

16. The apparatus according to claim 11 or 12, **characterized in that** said corrector (104, 154) is arranged for each of the plurality of areas.

17. The apparatus according to claim 11 or 12, **characterized in that**
each area of said image sensor (202, 213) has a plurality of pixel arrays which obtain different pieces of color information, and
said corrector (104, 154) is arranged for each color of each of the plurality of areas.

18. The apparatus according to claim 12 or 13, **characterized in that** said coefficient selector (1042) includes a register which outputs a coefficient.

19. The apparatus according to any one of claims 11 to 18, **characterized in that** said image sensor (202) is constituted by arraying in a predetermined direction a plurality of sensor chips (chip 1 - chip 16) on each of which a plurality of pixels are arrayed.

20. The apparatus according to any one of claims 11 to 18, **characterized in that** said image sensor (213) outputs signals from a plurality of pixels via output portions different between the plurality of areas.

21. The apparatus according to any one of claims 11 to 20, **characterized by further comprising** an imaging unit (2023, 210, 211, 212) which forms an image of an object to be sensed on said image sensor (202, 213), and a light source (2022, 209) which emits light.

22. The apparatus according to any one of claims 11 to 21, **characterized in that**
said image sensor (202, 213) reads at least one predetermined halftone image, and
the apparatus further comprises a calculation unit (108) which calculates coefficients used in said multiplier (1044) and said adder (1045) for each of the plurality of areas on the basis of a signal level of the read halftone image.

23. The apparatus according to claim 22, **characterized in that**
each area of said image sensor (202, 213) has a plurality of pixel arrays which obtain different pieces of color information, and
said calculation unit (108) calculates coefficients used in said multiplier (1044) and said adder (1045) for each color in each of the plurality of areas.

24. The apparatus according to any one of claims 11 to 23, **characterized in that** each area of said image sensor is formed from a sensor chip.

25. The apparatus according to any one of claims 11 to 24, **characterized in that** signals from the plurality of areas of said image sensor are output via different output systems.

26. An image forming apparatus **characterized by** comprising:

the image processing apparatus defined in any one of claims 1 to 25; and
a printer which prints an image on a sheet on the basis of a signal output from the image processing apparatus.

27. A correction method of correcting image data obtained from an image sensor formed from a plurality of areas each including a plurality of pixels, **characterized by** comprising the steps of:

reading a predetermined halftone image by the image sensor (S101);
selecting one of a plurality of correction data smaller in number than the plurality of areas for each of the plurality of areas on the basis of a signal level of the read image (S102 - S107);
storing correspondences between the plurality of areas and selected correction data (S108);
determining which of the areas outputs image data from the image sensor (S121); and
performing correction using correction data corresponding to the determined area (S122, S123).

28. The method according to claim 27, **characterized in that** the correction includes correction of decreasing a linearity difference between the plurality of areas.

29. A correction method of correcting image data obtained from an image sensor formed from a plurality of areas each including a plurality of pixels, **characterized by** comprising the steps of:

reading a predetermined halftone image by the image sensor (S201);
calculating a coefficient set used for correction for each of the plurality of areas on the basis of a signal level of the read image (S202);

EPODOC / EPO 19990582 1 >

storing correspondences between the plurality of areas and calculated coefficient sets (S203);
determining which of the areas outputs image data from the image sensor(S212);
selecting one of the stored coefficient sets on the basis of the determined area and the signal level of the image data (S213); and
correcting signals output from the plurality of areas by using coefficients of the selected coefficient set (S214),

wherein the correcting step includes:

a step of multiplying the signals output from the plurality of areas by the coefficients of the selected coefficient set; and
a step of adding the coefficients of the selected coefficient set to the signals output from the plurality of areas.

30. A computer readable program including instructions for controlling the processor to carry out the method of any one of claims 27 to 29.

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FIG. 1

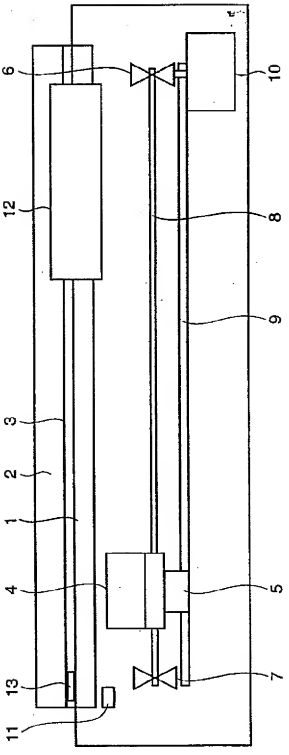

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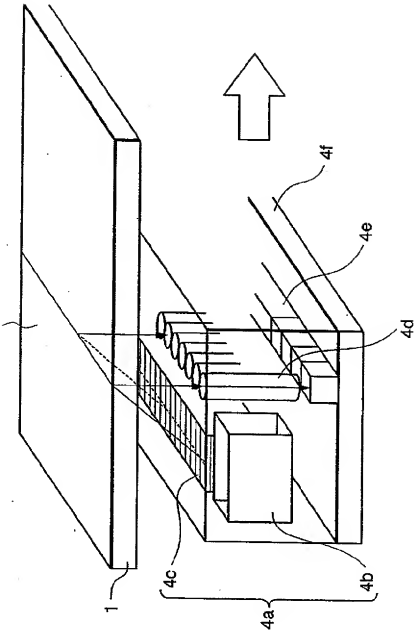
FIG. 2



EP 1 289 265 A2

FIG. 3

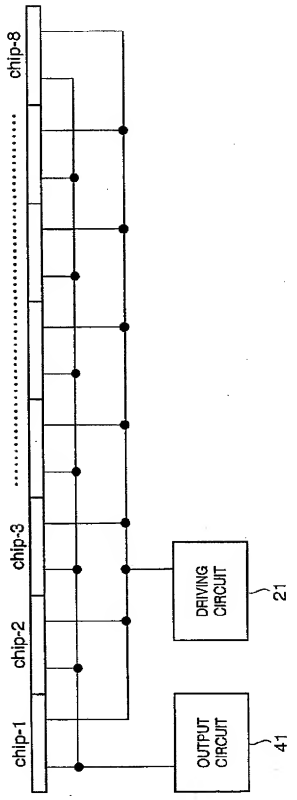
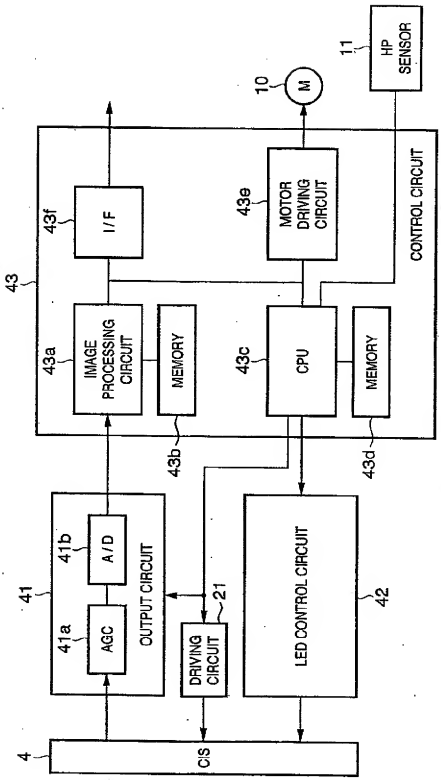

chip-8
chip-3
chip-2
chip-1
DRIVING CIRCUIT
21
OUTPUT CIRCUIT
41

FIG. 4



EDOCID: <EP_____1289265A2_I_>

FIG. 5

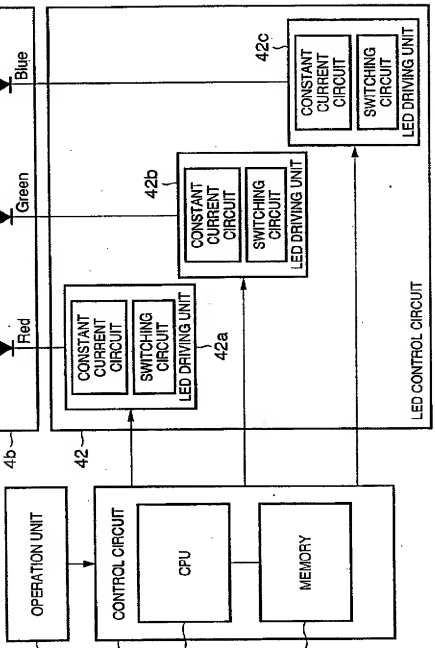

LED COMMON POWER SOURCE
LED LIGHT SOURCE UNIT
Red
Green
Blue
4b
42
OPERATION UNIT
12
CONTROL CIRCUIT
43
CPU
43c
MEMORY
43d
CONSTANT CURRENT CIRCUIT
SWITCHING CIRCUIT
LED DRIVING UNIT
42a
42b
42c
LED CONTROL CIRCUIT

FIG. 6

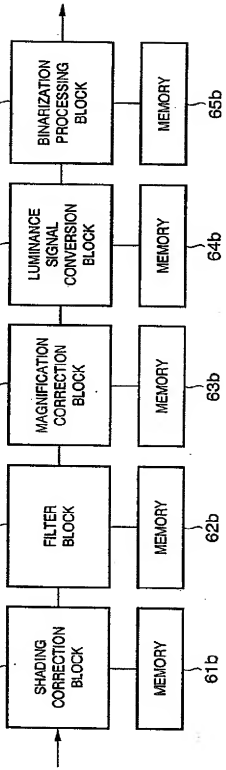


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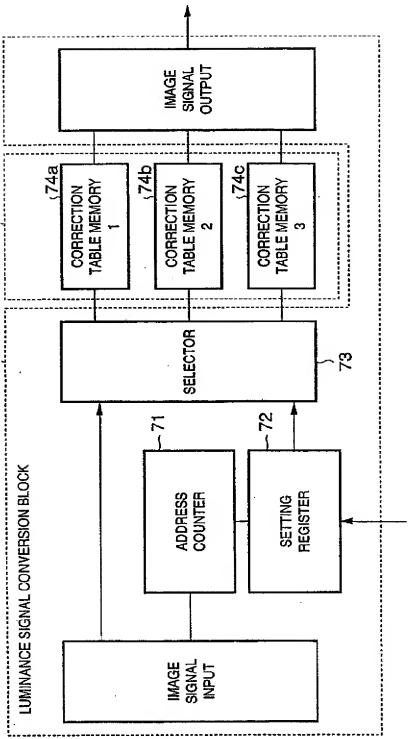
FIG. 7



BNSDOCID: <EP 1289265A2 1 >

FIG. 8

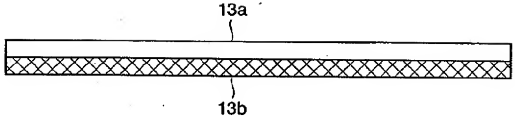


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FIG. 9A

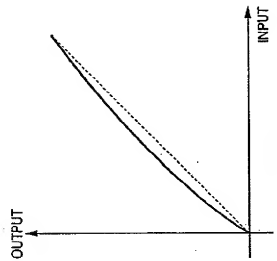

FIG. 9B

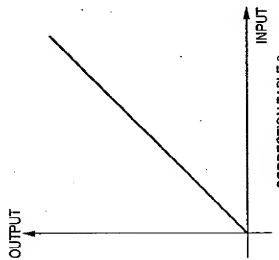

FIG. 9C

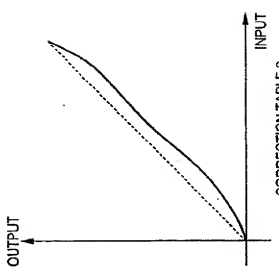

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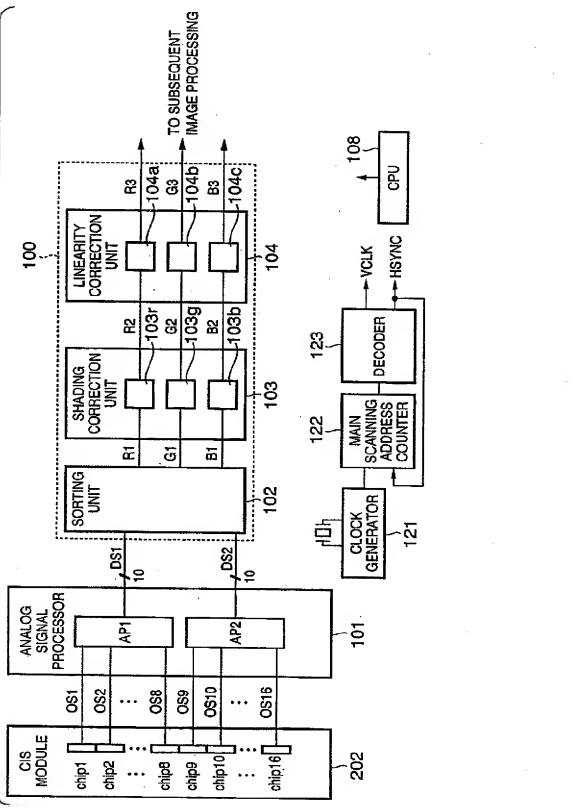
FIG. 10



SDOCID: <EP_____1289265A2_I_>

FIG. 11

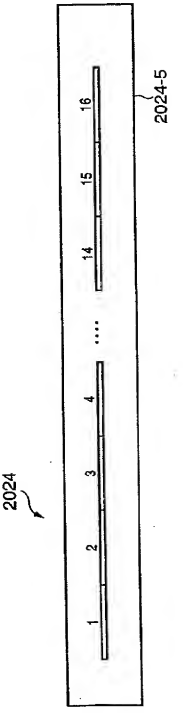


FIG. 12

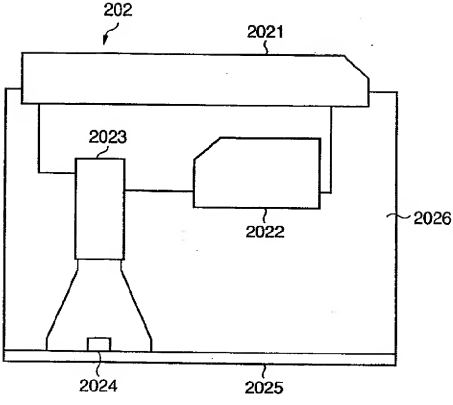


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FIG. 13

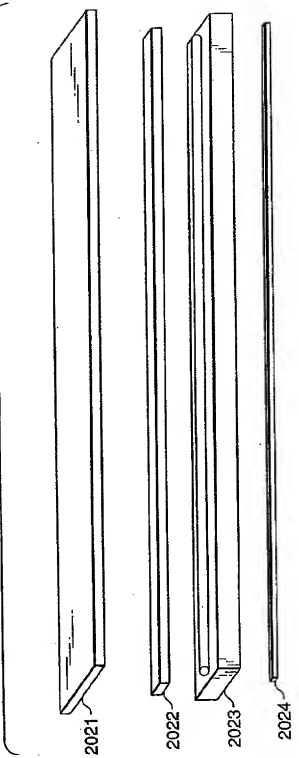
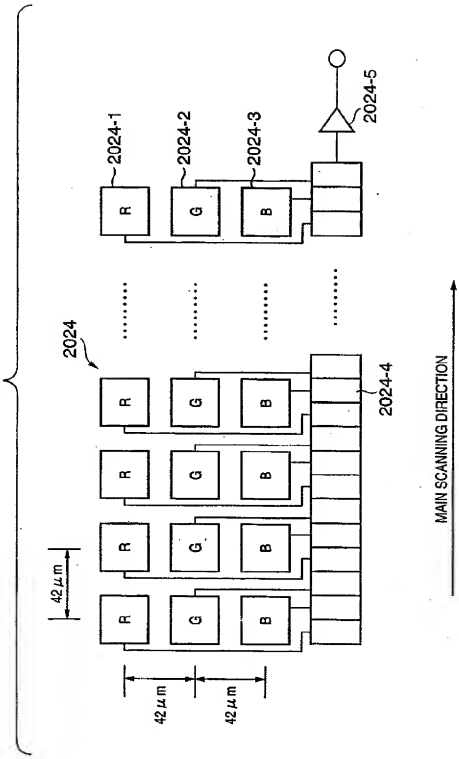


FIG. 14



IDOCID: <EP_____1289265A2_I_>

FIG. 15A

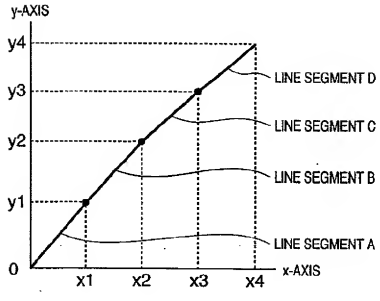


FIG. 15B

x-AXIS SECTION	SECTION n	COEFFICIENT A kn	COEFFICIENT B kn	CORRECTION FUNCTION
$0 \leq X < x1$	1	A1	B1	$Y = A1 * X + B1$
$x1 \leq X < x2$	2	A2	B2	$Y = A2 * X + B2$
$x2 \leq X < x3$	3	A3	B3	$Y = A3 * X + B3$
$x3 \leq X \leq x4$	4	A4	B4	$Y = A4 * X + B4$

FIG. 16

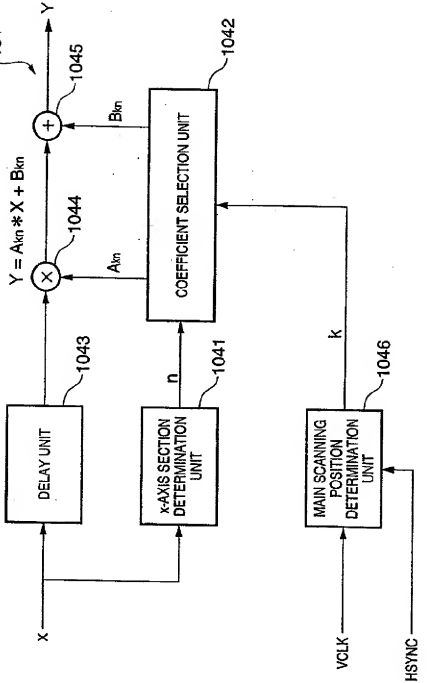


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FIG. 17

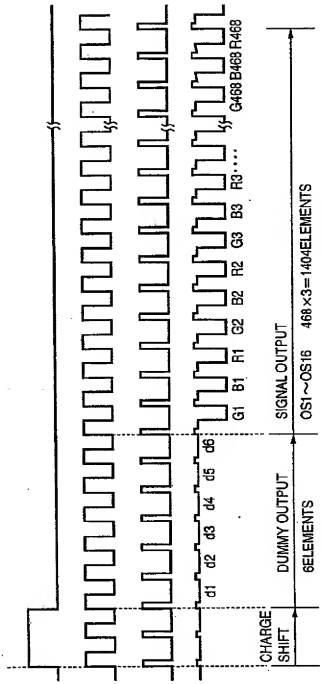
φSH
φM
φRS
OS1 ~OS16
CHARGE SHIFT
6ELEMENTS
d1 d2 d3 d4 d5 d6
DUMMY OUTPUT
G1 B1 R1 G2 B2 R2 G3 B3 R3 ··· G468 B468 R468
SIGNAL OUTPUT
OS1~OS16 468×3=1404ELEMENTS

FIG. 18

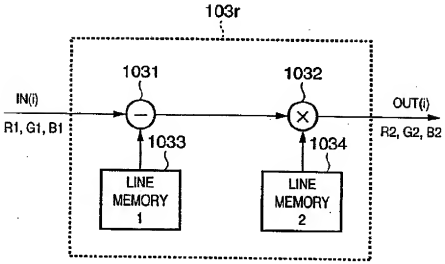

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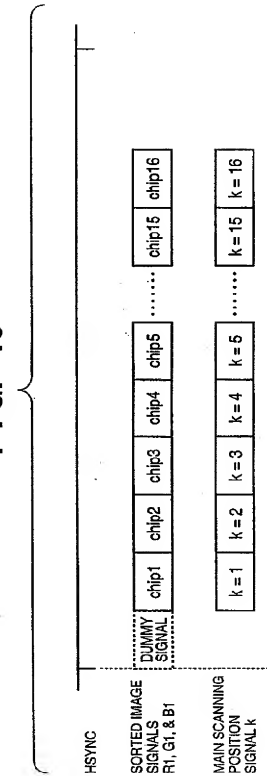
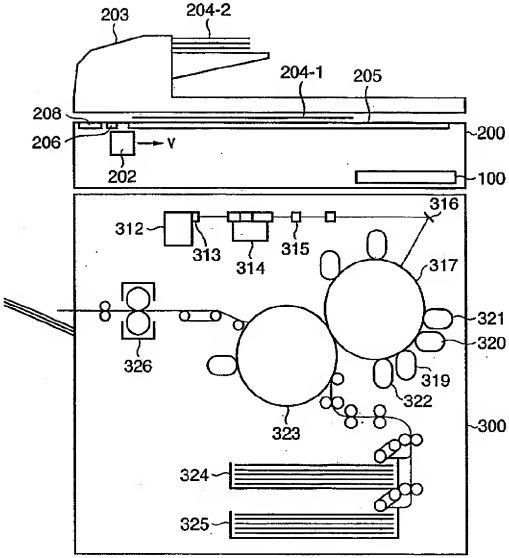
FIG. 19



EINSDOCID: <EP_____1289265A2_I_>

FIG. 20



\SDOCID: <EP_____1289265A2_I_>

FIG. 21

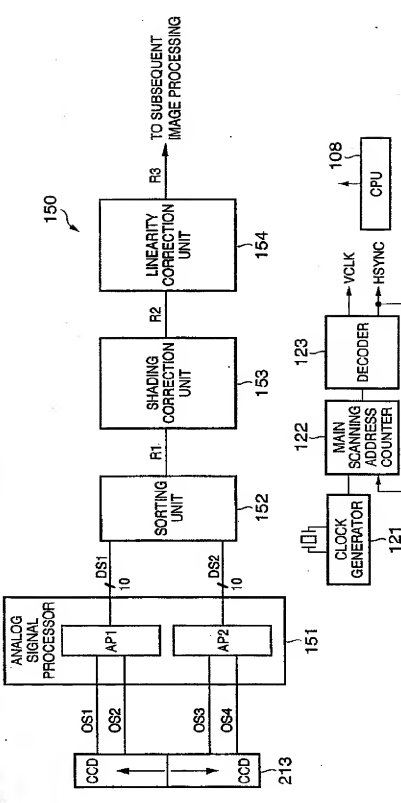


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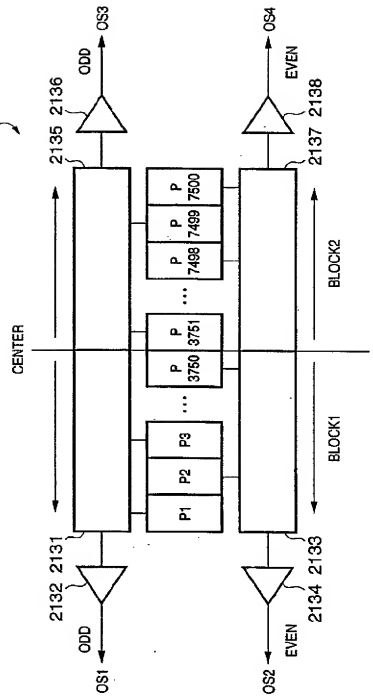
FIG. 22



ISOOCID: <EP_____1289265A2_I_>

FIG. 23

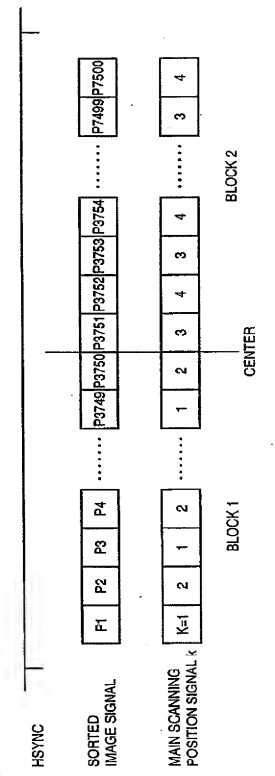


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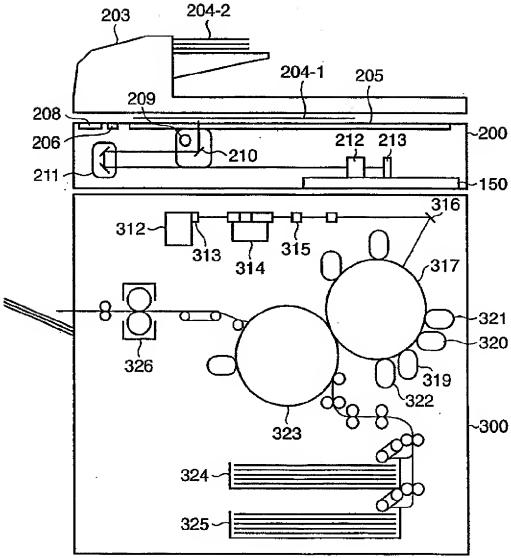
FIG. 24



\3DOCID <EP_____1289265A2_I_>

FIG. 25

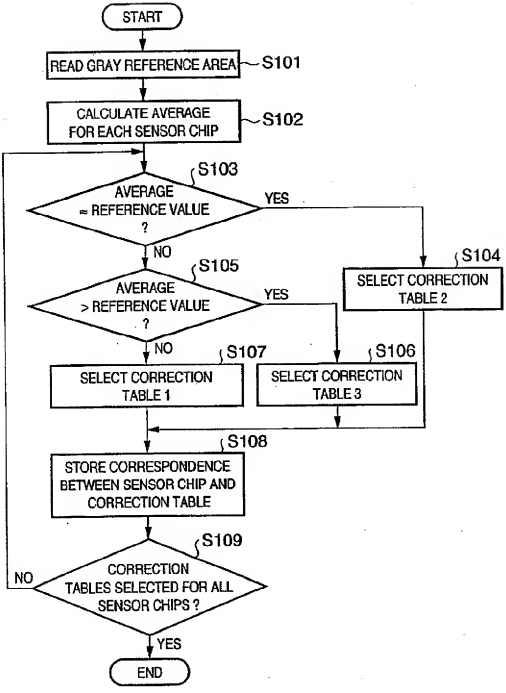
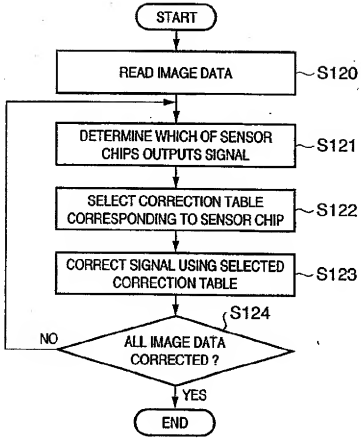
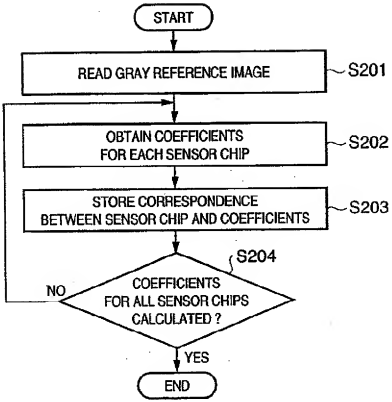

START
READ GRAY REFERENCE AREA
S101
CALCULATE AVERAGE FOR EACH SENSOR CHIP
S102
S103
AVERAGE ≈ REFERENCE VALUE ?
YES
NO
S104
SELECT CORRECTION TABLE 2
S105
AVERAGE > REFERENCE VALUE ?
YES
NO
S107
SELECT CORRECTION TABLE 1
S106
SELECT CORRECTION TABLE 3
S108
STORE CORRESPONDENCE BETWEEN SENSOR CHIP AND CORRECTION TABLE
S109
CORRECTION TABLES SELECTED FOR ALL SENSOR CHIPS ?
NO
YES
END

FIG. 26



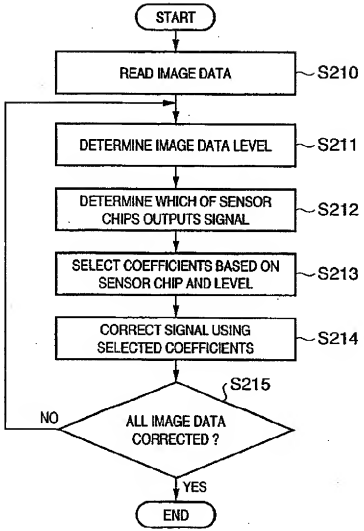
SOOCID: <EP_____1289265A2_I_>

FIG. 27



EP 1 289 265 A2

FIG. 28



SDOCID: <EP_____1289265A2_I_>

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 289 265 A3

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18.01.2002 JP 2002009741

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Bavariaring 4
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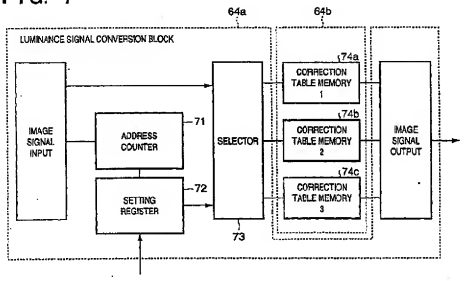
(54) Processing of signals from an image sensor consisting of a plurality of sensor areas

(57) An image processing apparatus includes an image sensor formed from a plurality of areas each including a plurality of pixels, and a corrector adapted to correct signals from the plurality of areas of the image sensor. The corrector has a plurality of correction data smaller in number than the areas, and performs correction by selectively using the correction data for each area of the image sensor.

FIG. 7



EP 1 289 265 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 01 8714

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 818 521 A (HIEDA TERUO) 6 October 1998 (1998-10-06) * column 5, line 45 - column 6, line 15 *	11,12, 15, 18-21, 24-26	H04N1/401
Y	KR 265 762 B (SAMSUNG ELECTRONICS CO LTD) 15 September 2000 (2000-09-15) * abstract *	11-26, 29,30	
L	-& US 6 573 934 B1 (JE-SUK LEE) 3 June 2003 (2003-06-03) translation of KR 265 762 B * the whole document *	11,26	
A	PATENT ABSTRACTS OF JAPAN vol. 0145, no. 84 (E-1018), 27 December 1990 (1990-12-27) & JP 2 254864 A (HITACHI LTD), 15 October 1990 (1990-10-15) * abstract *	1,4,27	
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